

FIG. 1

FIG. 2

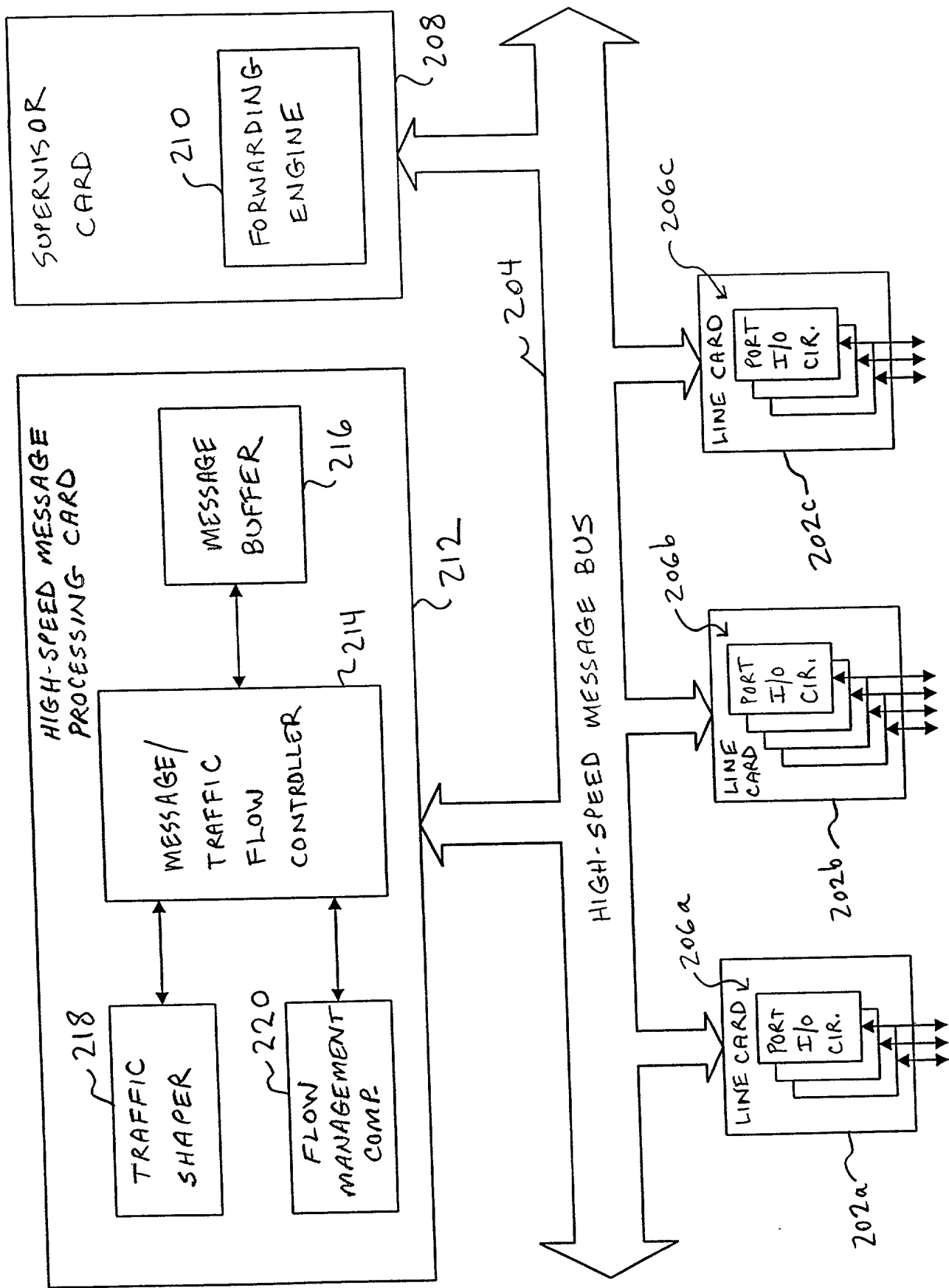


FIG. 2

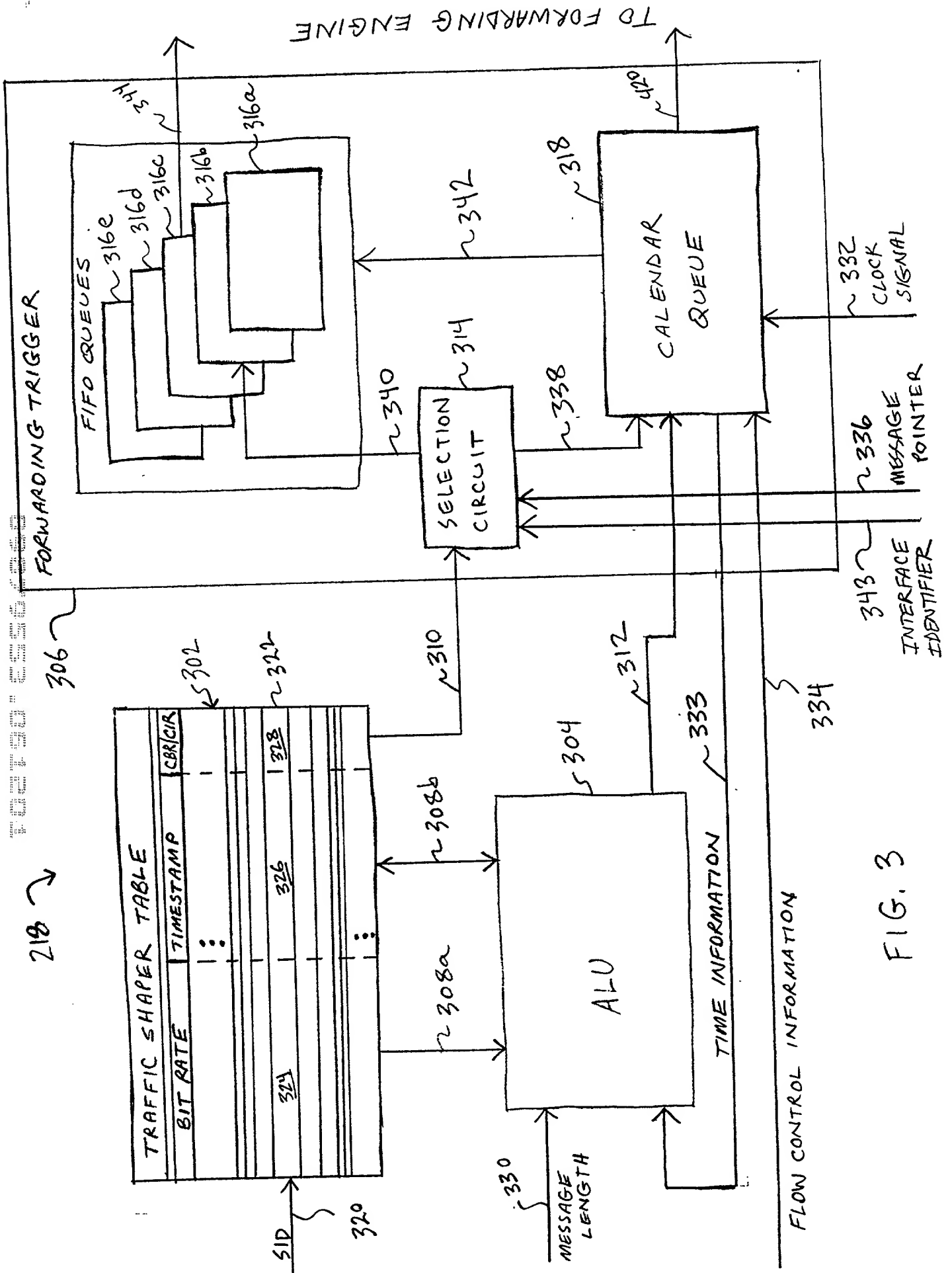


FIG. 3

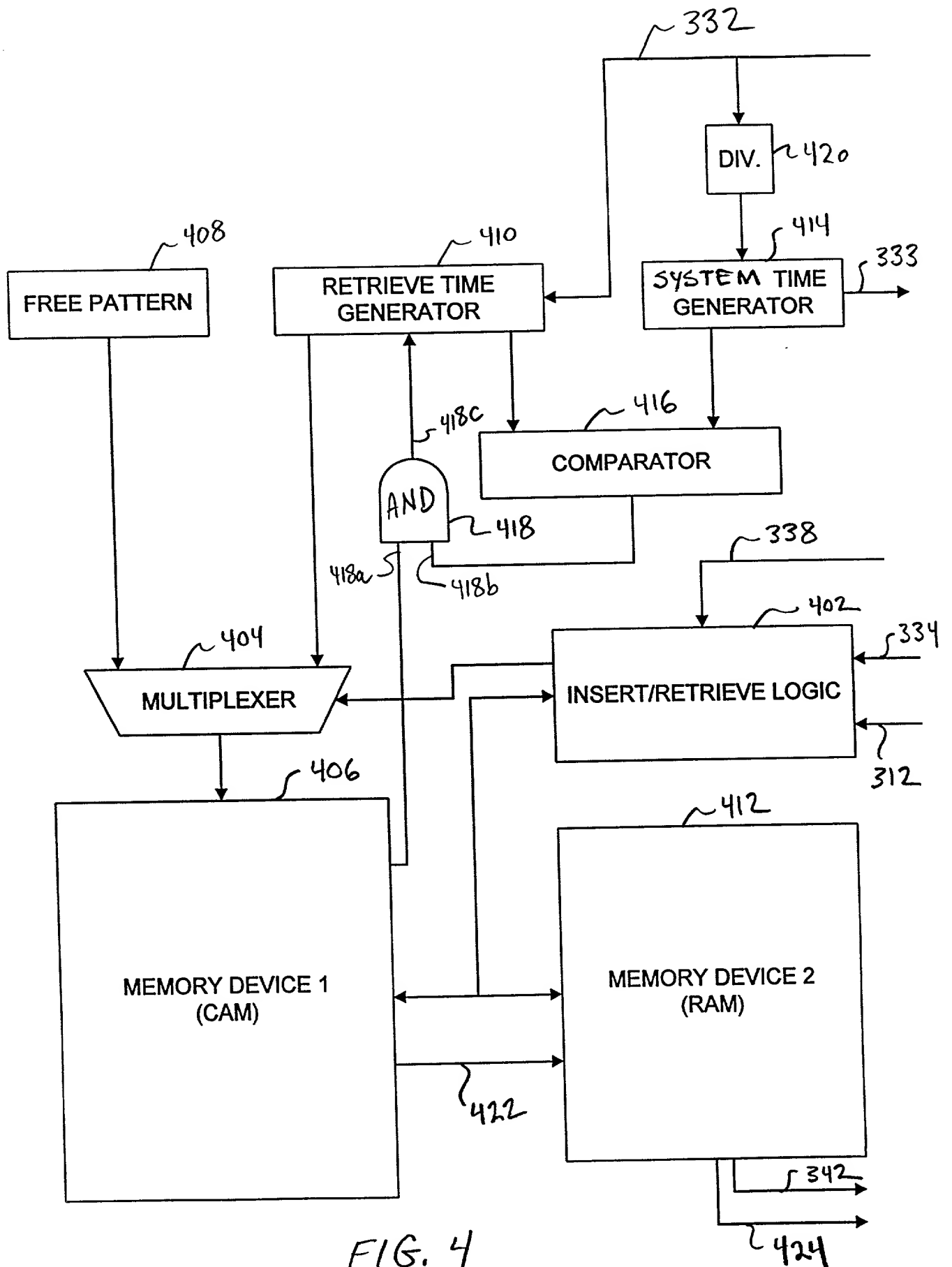


FIG. 4

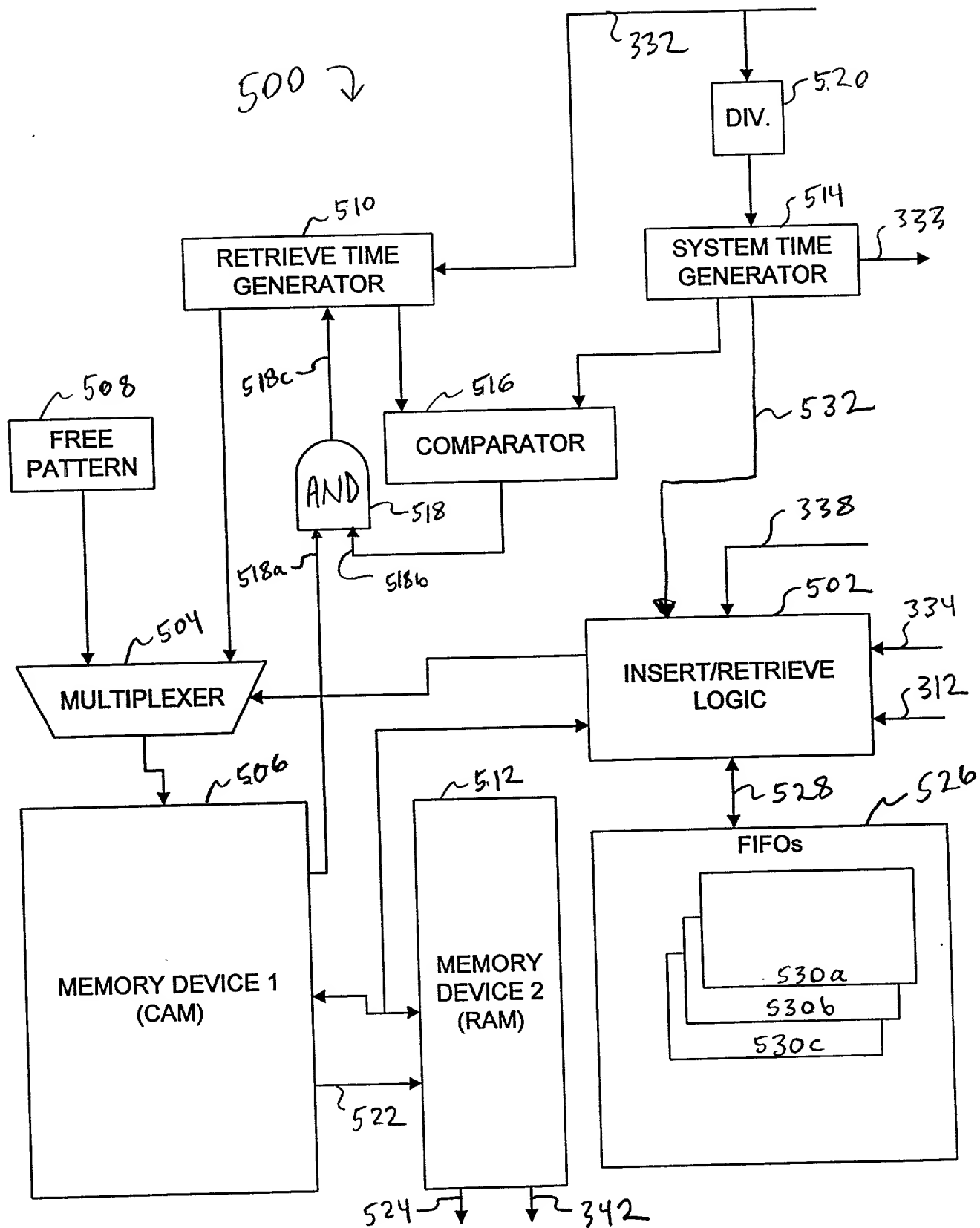
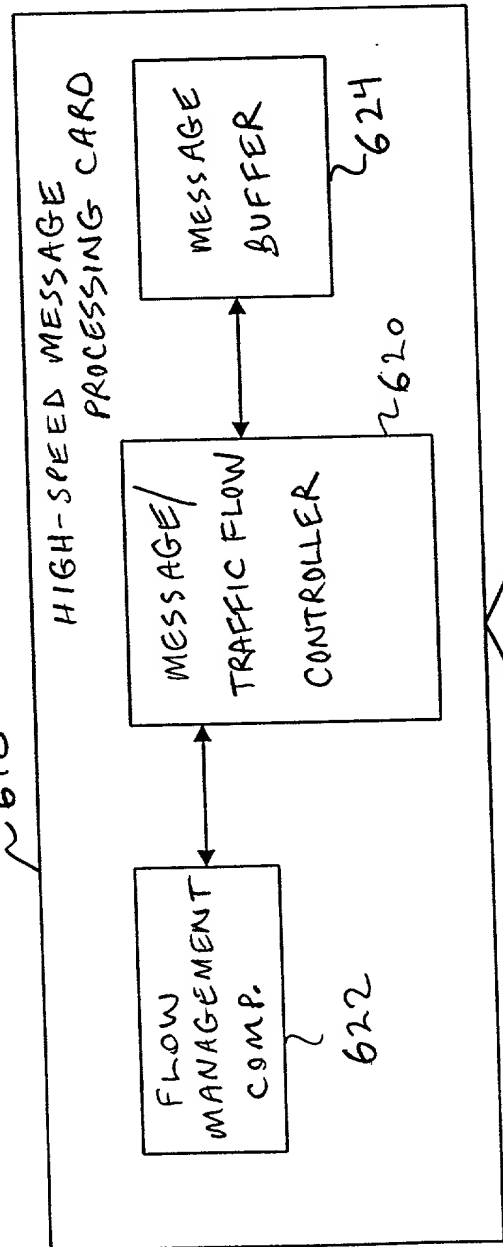


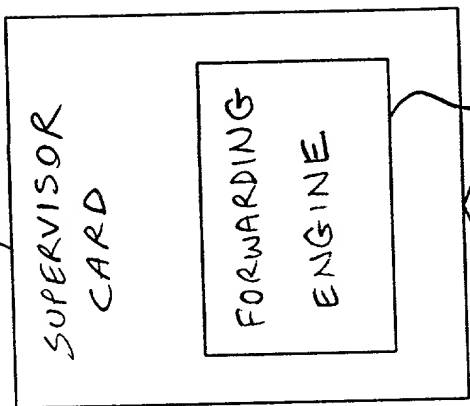
FIG. 5

FIG. 6

618



614



606

SWITCHING BUS

610c

610b

610a

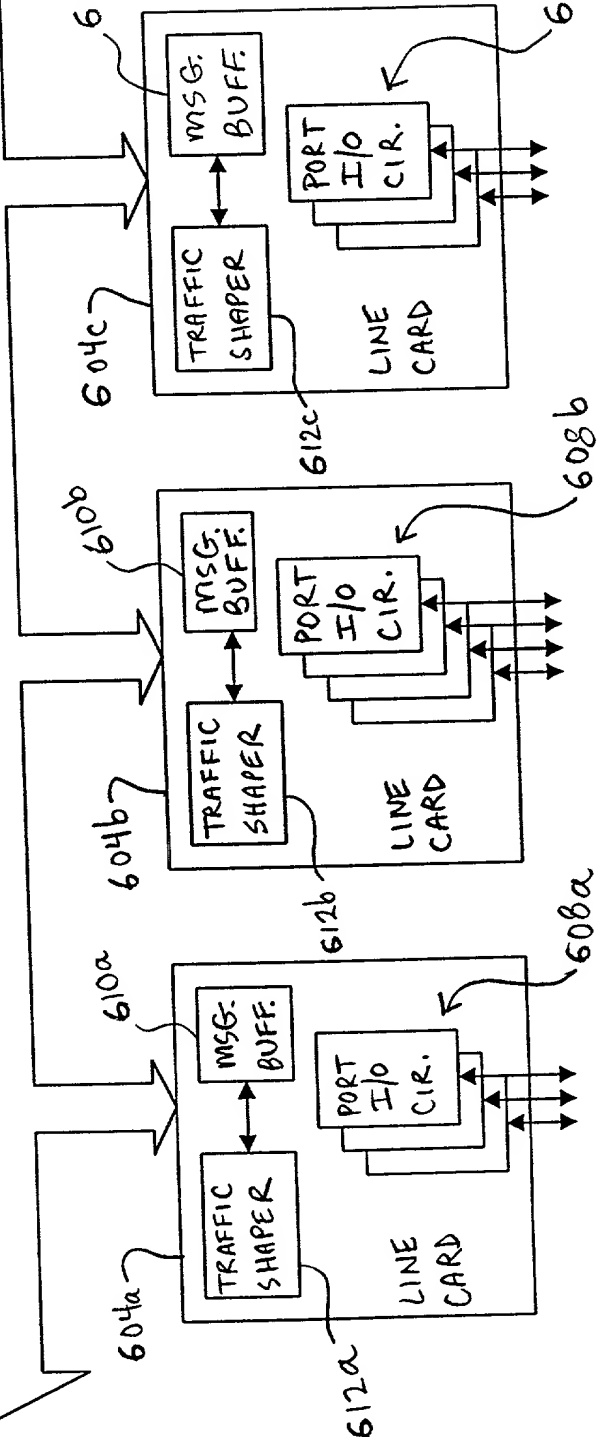


FIG. 6

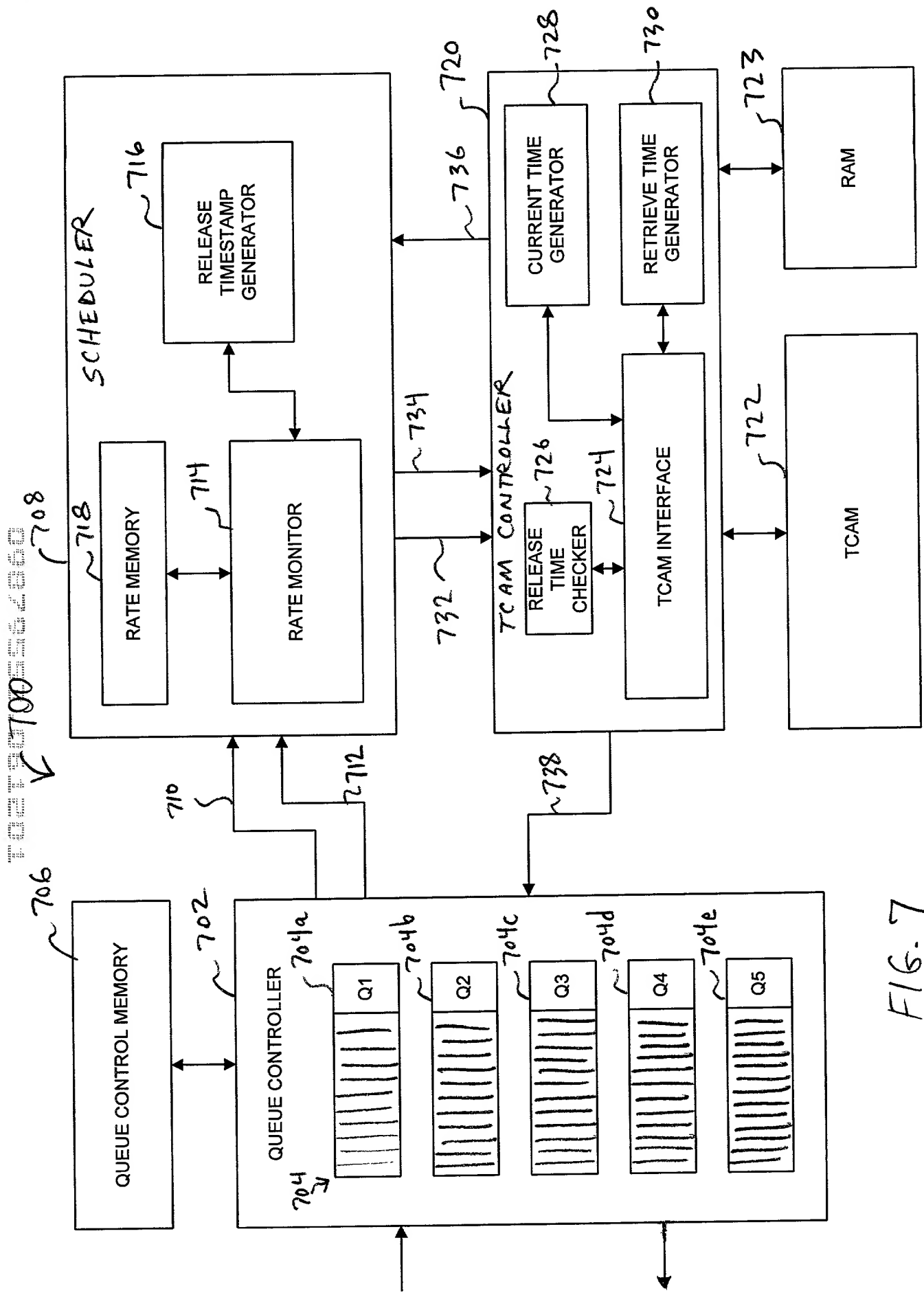


FIG. 7

QUEUE CONTROL MEMORY					
SID	Q No.	Qtime_Req	Head Ptr.	Tail Ptr.	Next SID
814a ~	Q1	0			
814b ~	Q2	0			
814c ~	Q3	1			
814d ~	Q4	1			
814e ~	Q5	0			
814f ~	Q6	1			
814g ~	Q7	1			
814h ~	Q8	1			

FIG. 8

RATE MEMORY							
next SID	Last Updated Time	Drain Rate	Last Updated Level	High Water Mark Threshold	Low Water Mark Threshold	CIR Rate	EIR Rate
918a ~							
918b ~							
918c ~							
918d ~							
918e ~							
918f ~							
918g ~							
918h ~							

FIG. 9

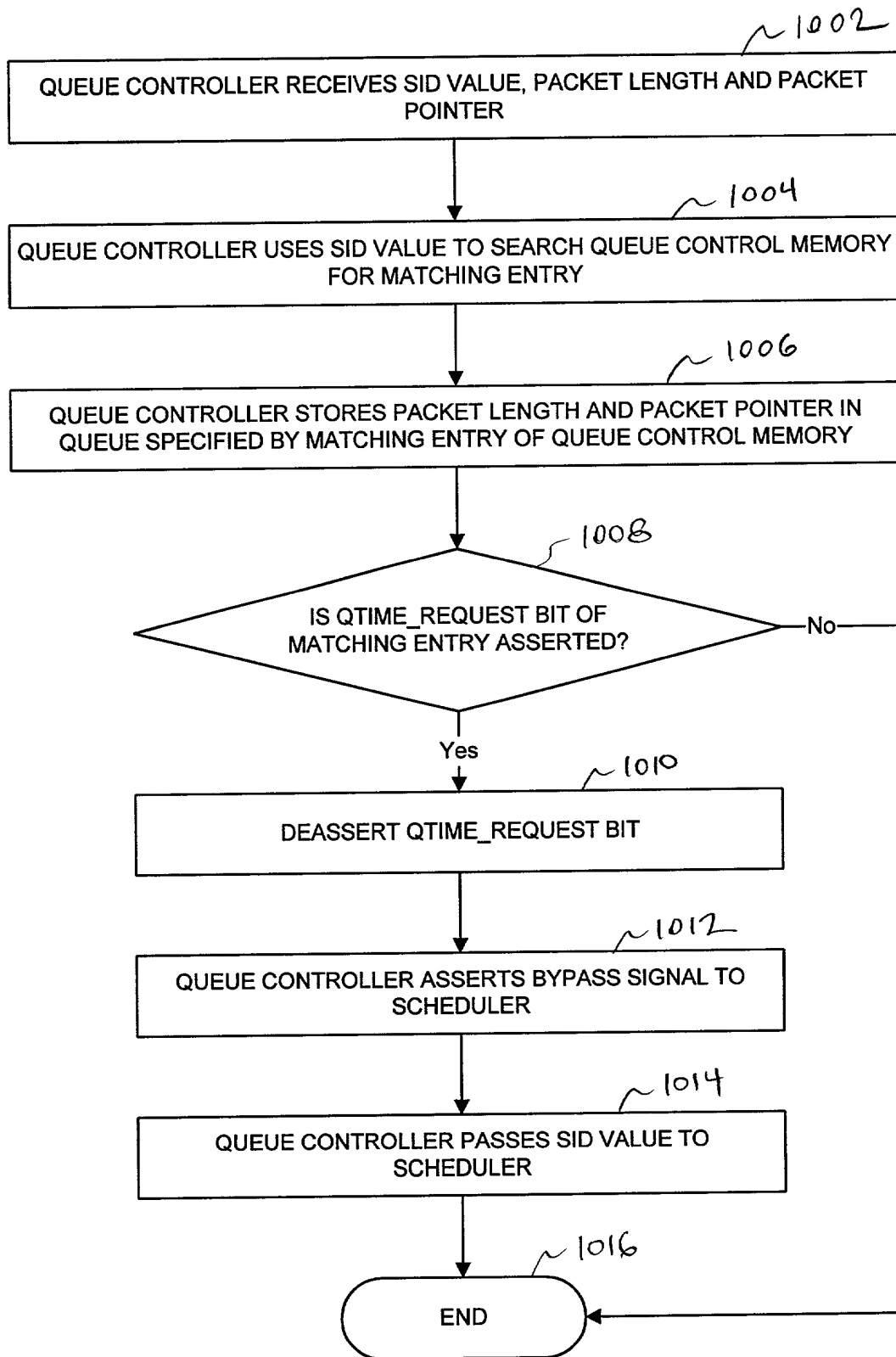


FIG. 10A

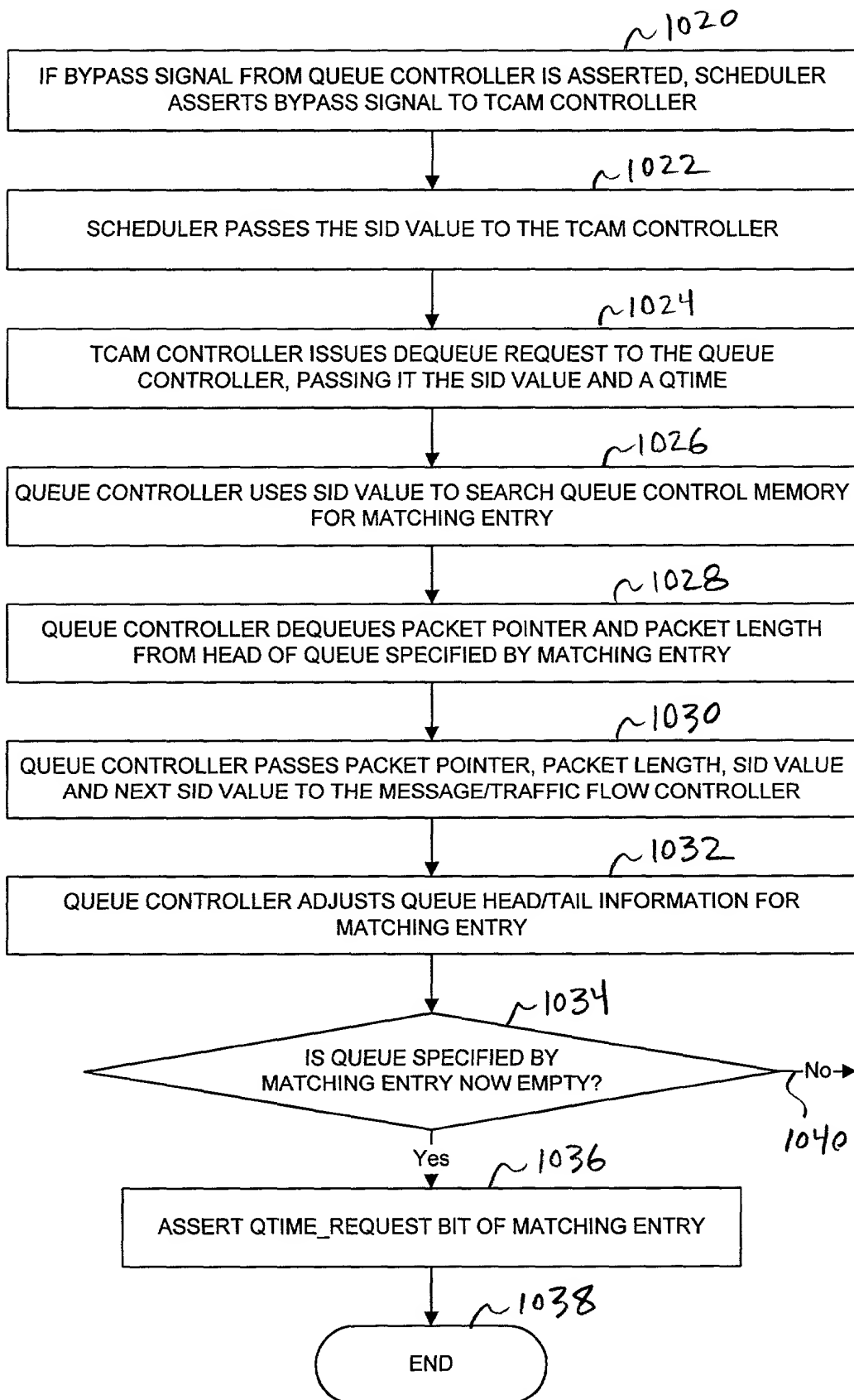
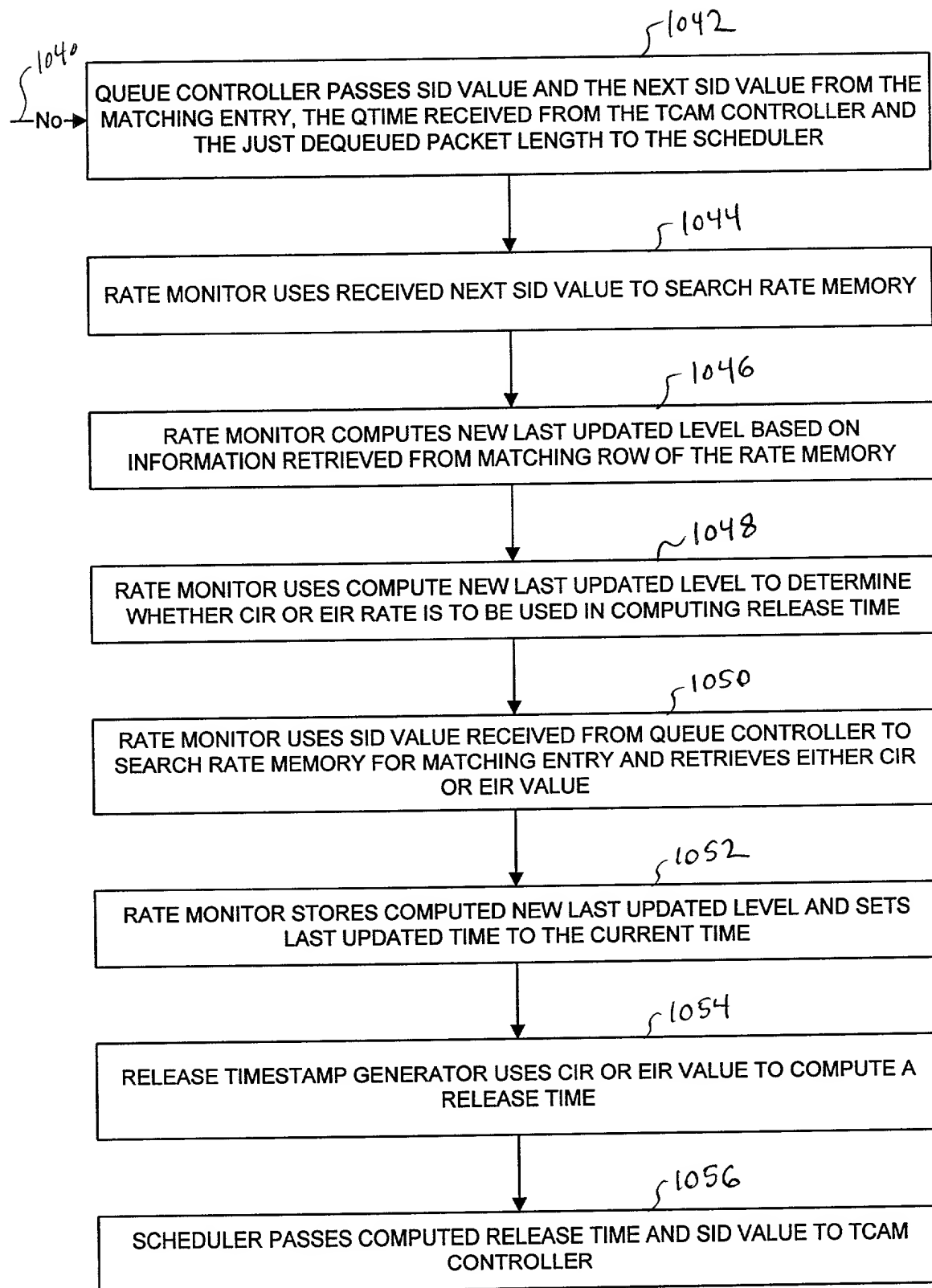


FIG. 10B



TO FIG.
10D

FIG. 10C

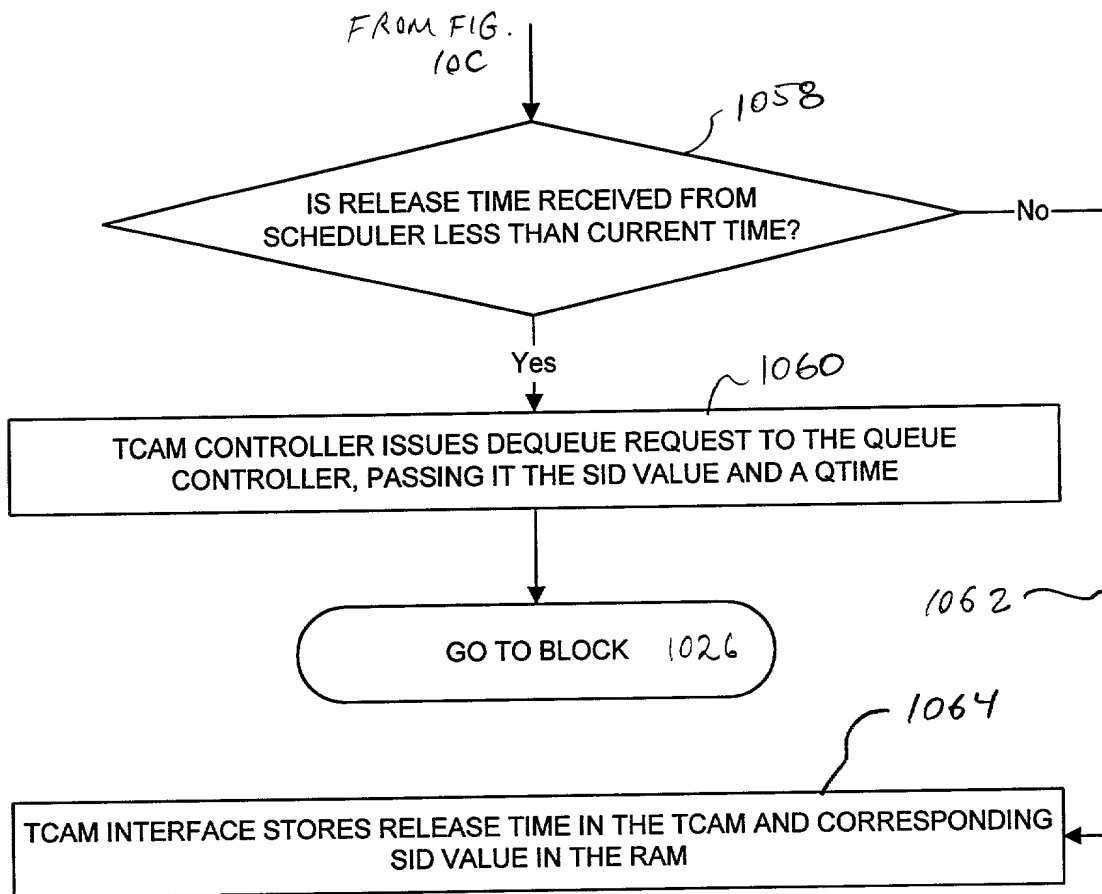
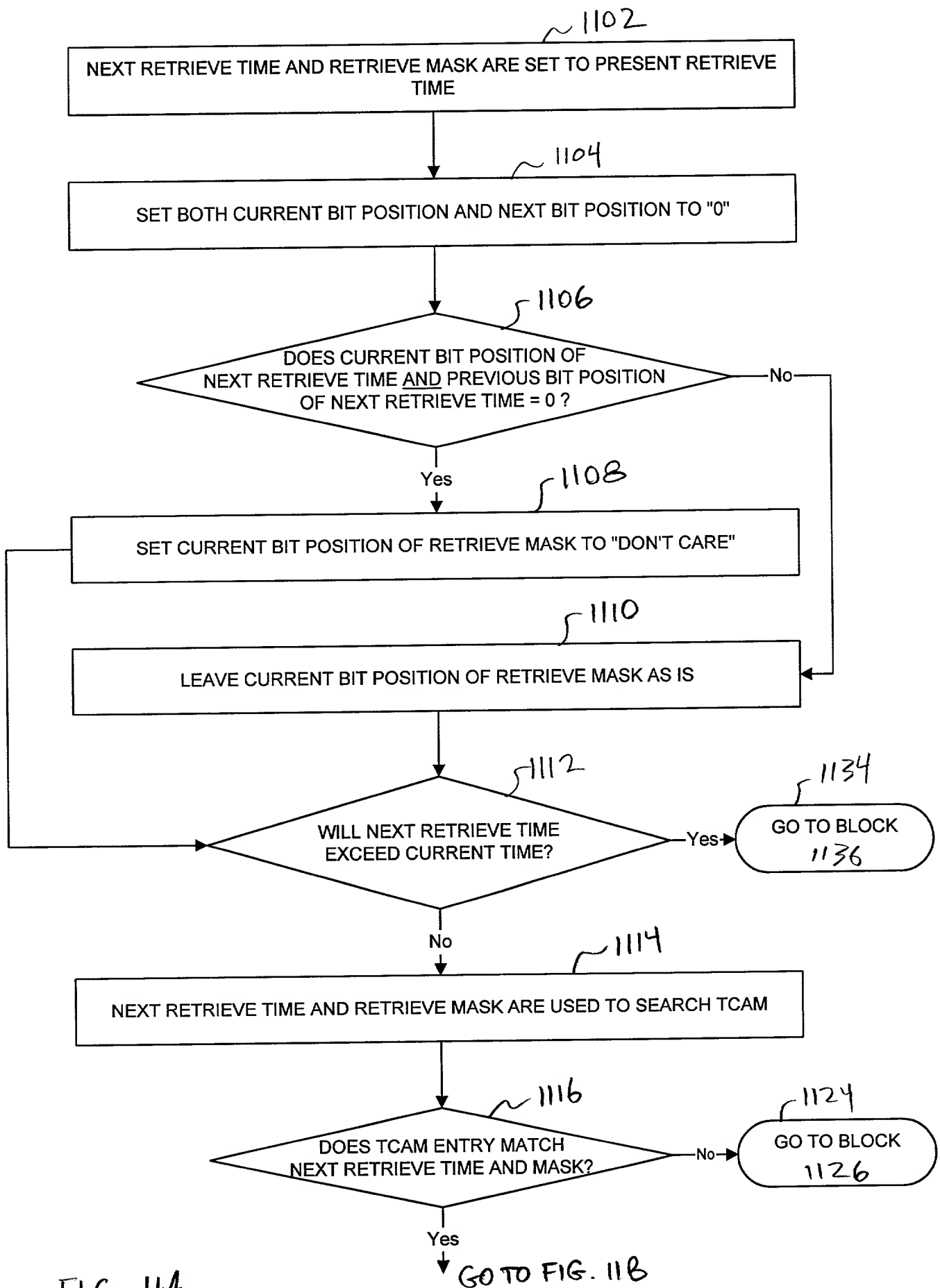


FIG. 10D



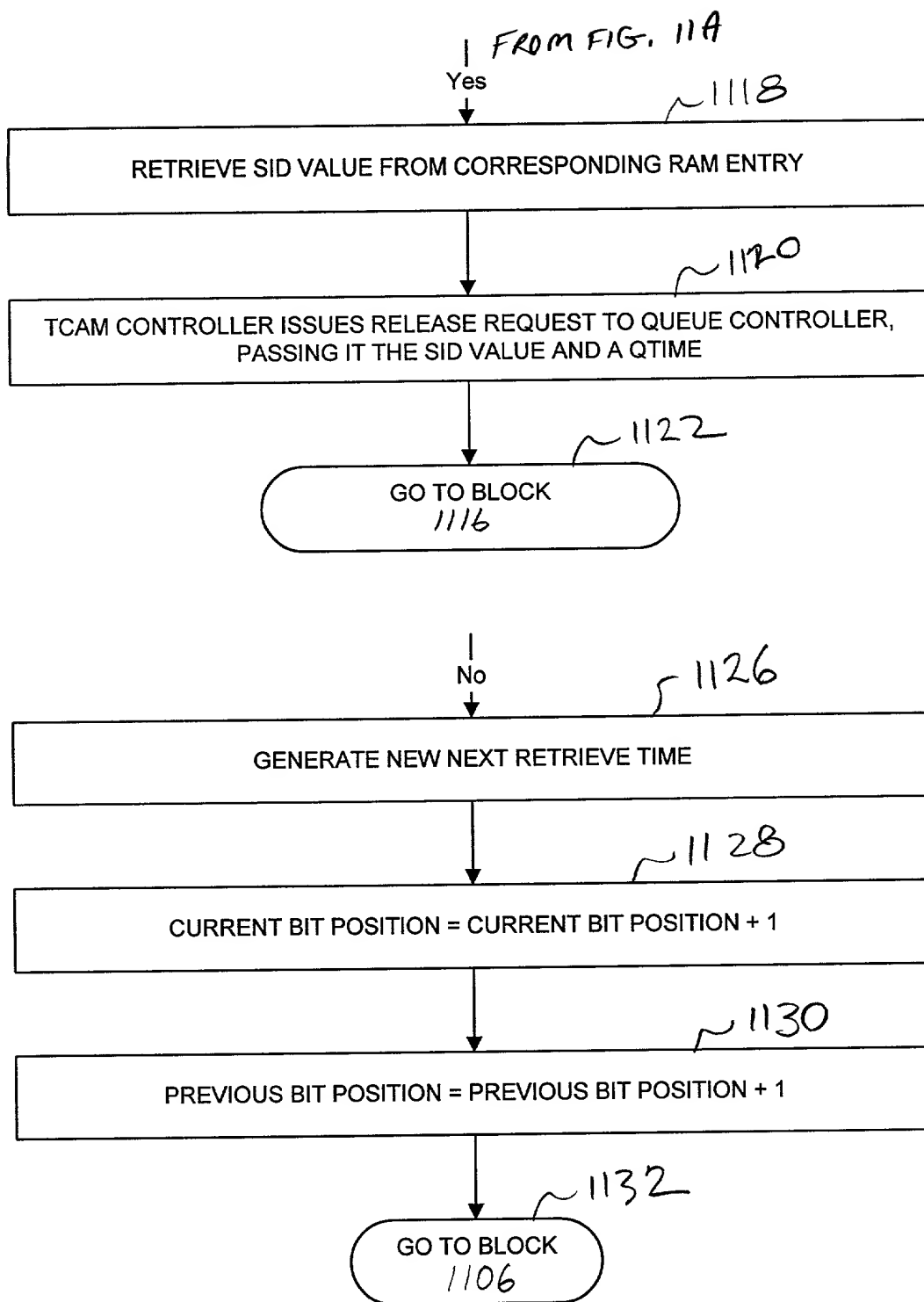


FIG. 11B

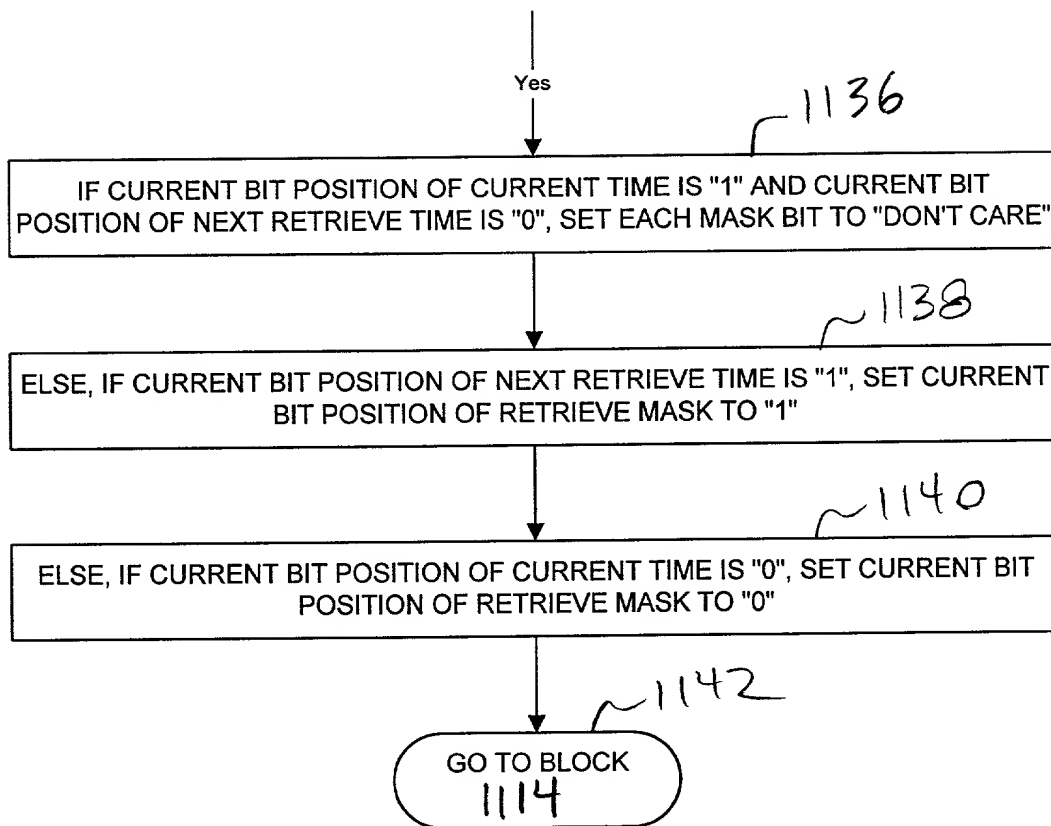


FIG. 11C